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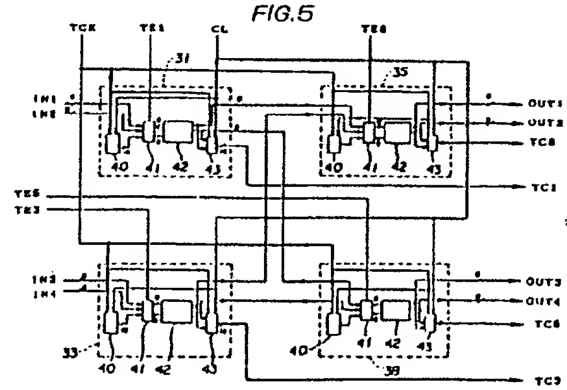
The title of the invention has been amended (Guidelines for Examination in the EPO, A-III, 7.3).

(54) **Semiconductor integrated circuit with a test function.**

(57) A semiconductor integrated circuit comprises a plurality of integrated circuit blocks (31 - 39) constituted on a wafer (30), the integrated circuit blocks being arbitrarily electrically connected to each other so as to form a system. Each of the integrated circuit blocks comprises a logical operating circuit (42) for carrying out a logical operation; a pseudo-random pattern generating circuit (40) for generating a pseudo-random pattern signal; switching circuit (41) for selecting either an input signal to be processed by the logical operating circuit or the pseudo-random pattern signal in response to a test enabling signal (TE1 - TE9) which is independently applied to each integrated circuit block so that each integrated circuit block is independently set to either a test mode or a normal mode and for outputting the selected signal to the logical operating circuit; and a data compressing circuit (43) for compressing an output data signal of the logical operating circuit.

FIG.5



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description when read in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a block diagram of an integrated circuit block of a conventional semiconductor integrated circuit;

FIGS.2(A) through 2(C) are timing charts of signals used in the block structure shown in FIG.1;

FIG.3A is a block diagram of a conventional semiconductor integrated circuit in which a system is constituted by the combination of a plurality of integrated circuit blocks each having the configuration shown in FIG.1;

FIG.3B is a block diagram of a pseudo-random pattern generator shown in FIG.3A for a system test;

FIG.4 is a block diagram of an example of a semiconductor integrated circuit according to the present invention in which a system is constituted by a plurality of integrated circuit blocks;

FIG.5 is a detailed block diagram of the system shown in FIG.4;

FIGS.6(A) through 6(C) are timing charts of signals used in the configuration shown in FIGS.4 and 5;

FIG.7 is a circuit diagram of a pseudo-random pattern generator shown in FIG.5;

FIG.8 is a circuit diagram of a switching circuit shown in FIG.5;

FIG.9 is a circuit diagram of a 1-bit switching circuit of the switching circuit shown in FIG.8; and

FIG.10 is a circuit diagram of a data compressor shown in FIG.5.

DETAILED DESCRIPTION

A description will first be given on a conventional wafer-scale integrated circuit for a better understanding of the present invention.

FIG.1 is a block diagram of an example of one integrated circuit block of a conventional wafer-scale integrated circuit. An integrated circuit block 11 is composed of a pseudo-random pattern generator 12, a switching circuit 13, a butterfly processor 14 and a data compressor 15. The pseudo-random pattern generator 12 and the data compressor 15 constitutes a self-testing circuit for the block 11. The pseudo-random pattern generator 12 generates a pseudo-random pattern Ti for testing the integrated circuit block 11 by use of a clock signal TCK for tests. In this example, the pseudo-random pattern is made up of 16 bits. The generator 12 is cleared by the clear signal CL. The switching circuit 13 selects either two 8-bit input signals from an integrated circuit block followed by the block 11 (or an external circuit) or the output signal from the generator 12 in response to a test enabling signal TE. The butterfly processor 14 has a pair of 8-bit input lines and a pair of 8-bit output lines and executes butterfly computation. Output signals of the butterfly processor are fed to following integrated circuit blocks or an external circuit. Also, the output signals of the butterfly processor 14 are fed to the data compressor 15, which compresses the received signal and produces a compressed data (a signature output) TC of 16 bits in synchronization with the test clock signal TCK. The compressed data is outputted to the external circuit. The data compressor 15 is cleared in response to the clear signal CL.

A description will be given on the operation upon the self-test of the integrated circuit block, by referring to FIG.2.

First of all, the clear signal CL and the test enabling signal TE produced by a testing circuit (not shown) are set to a high level as shown in FIGS.2(A) and 2(B), respectively. Then, the pseudo-random pattern generator 12 and the data compressor 15 are initially set, and the switching circuit 13 selects the output signal Ti of the generator 12. Then, the test clock signal TCK shown in FIG.2(C) is supplied to the pseudo-random pattern generator 12 and the data compressor 15. The pseudo-random pattern is passed through the switching circuit 13 and fed to the butterfly processor 14, the output of which is supplied to the data compressor 15. Then, the compressed data (the signature output) from the data compressor 15 is compared with an expected value data by the test device. If the integrated circuit block is non-defective, both the data are identical to each other. In the same way, the other integrated circuit blocks can be tested.

Integrated circuit blocks which are discriminated against the defective integrated circuit blocks may be electrically coupled so as to constitute a desired system. As described before, the system composed of the integrated circuit blocks must be tested to check whether or not the system is defective. For this purpose, a self-testing circuit for the system test is added to the conventional wafer-scale integrated circuits.

FIG.3A is a block diagram of a conventional semiconductor integrated circuit of the wafer scale having a self-testing circuit for the system test. Integrated circuit blocks 17 to 25 each having the structure shown in FIG.1 are formed on a wafer 16. In this configuration, it is assumed that the integrated circuit blocks 17, 19, 21 and 24 are non-defective and the other blocks are defective. The non-defective integrated circuit blocks are electrically connected by signal lines 28a, 28b, 28c and 28d, as shown in FIG.3A, and thus a system of a 4-point fast Fourier transform (hereafter referred to as FFT) processor is constituted. The test enabling signal TE, the clear signal CL and the test clock signal TCK are commonly supplied to the integrated circuit blocks 17 to 25. TC1 to TC9 denote compressed data from the corresponding integrated circuit blocks.

A block 26 denotes a pseudo-random pattern generator which is added to the system in order to test the operation of the FFT processor composed of the blocks 17, 19, 21 and 24. A detailed configuration of the pseudo-random pattern generator 26 is illustrated in FIG.3B. The generator 26 consists of a pseudo-random pattern generator 26a and a switching circuit 26b for selecting either four 8-bit input signals IN1 to IN4 or four 8-bit pseudo-

the blocks 31 and 33 are passed through the switching circuits 40 and fed to the butterfly processors 42 in the blocks 35 and 38. Then, the output signals of the processors 42 are fed to the data compressors 43. Even when the blocks 35 and 38 are in the normal operating mode, the generator 40 and the compressor 43 are active.

Next, the test clock signal TCK is activated as shown in FIG.6(D). Then, the pseudo-random pattern generator 40 and the data compressor 43 of each block start to operate. Since the blocks 31 and 33 are maintained in the test mode, the pseudo-random pattern signals from the generators 40 thereof are passed through the switching circuits 41 and fed to the butterfly processors 42. The output signals of the butterfly processors 42 of the blocks 31 and 33 are fed to the integrated circuit blocks 35 and 38. The signals from the blocks 31 and 33 are passed through the switching circuits 41 of the blocks 35 and 38, respectively, and fed to the butterfly processors 42 thereof. Then, the output signals of the processors 42 of the blocks 35 and 38 are delivered to the data compressors 43 thereof, so that the compressed data (signature outputs) TC5 and TC8 are outputted through the output terminals (not shown) to the test device.

After a predetermined number of the test clock signal TCK is applied to the system, the compressed data derived from the blocks 35 and 38 are compared with an expected value data. If the system is not defective, both the data are identical to each other. In this way, it is possible to check the operation of the system by using the self-testing circuits each composed of the pseudo-random pattern generator and the data compressor built-in the integrated circuit blocks. Therefore, the additional self-testing circuit for the system test provided on the wafer is no longer necessary to check the operation of the system.

FIG.7 is a circuit diagram of the pseudo-random pattern generator 40 shown in FIG.5. As shown, the generator 40 consists of 15 delayed flip-flop circuits F1 to F15 with clear terminals, 1 delayed flip-flop F16 with a set terminal, and 3 exclusive-OR circuits E-OR. For simplicity, the test clock signal TCK and the clear signal CL are not illustrated. The pseudo-random pattern of 16 bits t1 to t16 is obtained at the output terminals of the flip-flop circuits F1 to F16. The structure shown in FIG.7 is so-called a linear feedback shift register producing a cyclic redundancy check signal.

FIG.8 is a detailed block diagram of the switching circuit 41. The switching circuit 41 is composed of sixteen 1-bit switching circuits illustrated with rectangular blocks. Symbols a1 to a16 denote bits of the input signal. Input bits of the switching circuit 41 are represented by i1 to i16.

FIG.9 is a circuit diagram of one 1-bit switching circuit. The 1-bit input signal a1 and 1-bit pattern signal t1 are inverted by inverters 41a and 41b and fed to transmission gates 41f and 41g, respectively. The transmission gates 41f and 41g are controlled by both the test enabling signal TE1 and an inverted test enabling signal. When one of the gates is in a closed state, the other is in an open state. The output signals of the gates 41f and 41g are inverted by an inverter 41d and fed to the butterfly processor 42.

FIG.10 is a circuit diagram of the data compressor 43. As illustrated, the data compressor 43 consists of 16 delayed flip-flop circuits F1 to F16 with clear terminals and 19 exclusive-OR circuits E-OR. For simplicity, the test clock signal TCK and the clear signal CL are not shown. Symbols tc1 to tc16 denote bits of the compressed data.

The present invention is not limited to the embodiment described in the foregoing, but various variations and modifications may be made without departing the scope of the present invention. For example, the present invention is not limited to the butterfly processor. Any logical operation for the integrated circuit block is applicable. The system may be constituted with combinations of the same kind of the integrated circuit blocks or different kinds of the integrated circuit blocks. Moreover, even when a plurality of systems are constituted in the semiconductor integrated circuit, these systems may be tested in the same manner as that described in the foregoing.

Claims

1. A semiconductor integrated circuit including a plurality of integrated circuit blocks (31 - 39) constituted on a wafer (30), said integrated circuit blocks being arbitrarily electrically connected to each other so as to form a system, each of said integrated circuit blocks comprising logical operating means (42) for carrying out a logical operation; pseudo-random pattern generating means (40) for generating a pseudo-random pattern signal; and data compressing means (43) for compressing an output data signal of said logical operating means, characterized in that each of said integrated circuit blocks further comprises switching means (41) for selecting either an input signal to be processed by said logical operating means or said pseudo-random pattern signal in response to a test enabling signal (TE1 - TE9) which is independently applied to each integrated circuit block so that each integrated circuit block is independently set to either a test mode or a normal operating mode, and for outputting the selected signal to said logical operating means.

2. A semiconductor integrated circuit as claimed in claim 1, characterized in that at the time of testing said system, said switching means of each of integrated circuit blocks (31, 33) positioned at first stage of said system is controlled by the test enabling signal so as to select the pseudo-random pattern, and said switching means of each of integrated circuit blocks (35, 38) other than the blocks at the first stage is controlled by the test enabling signal so as to select the input signals.

3. A semiconductor integrated circuit as

FIG. 1 (PRIOR ART)

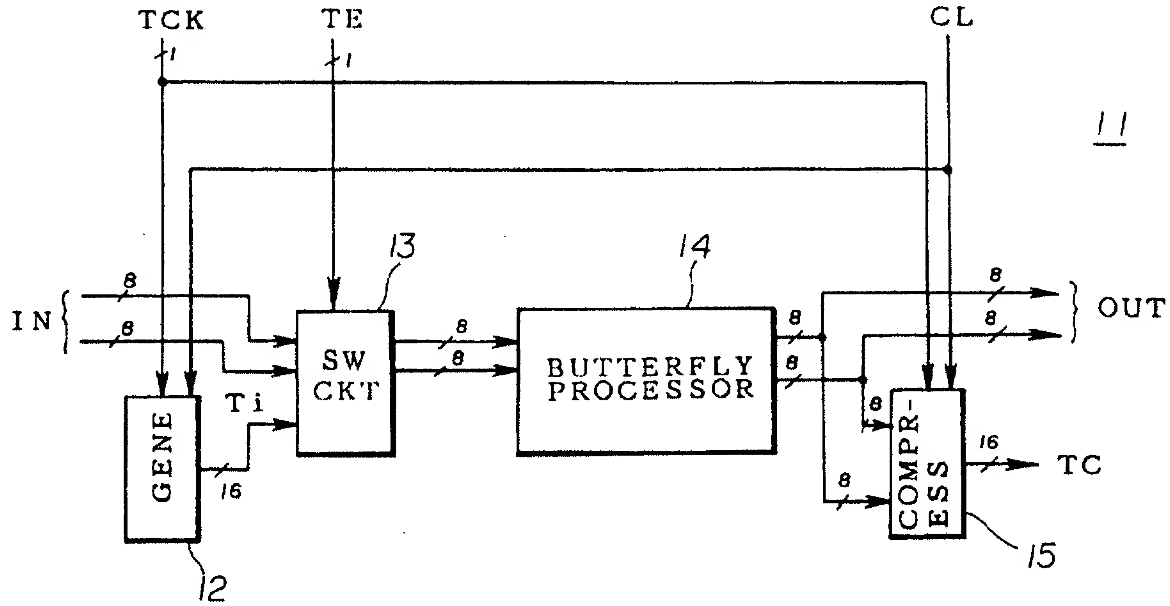

FIG.2 (PRIOR ART)

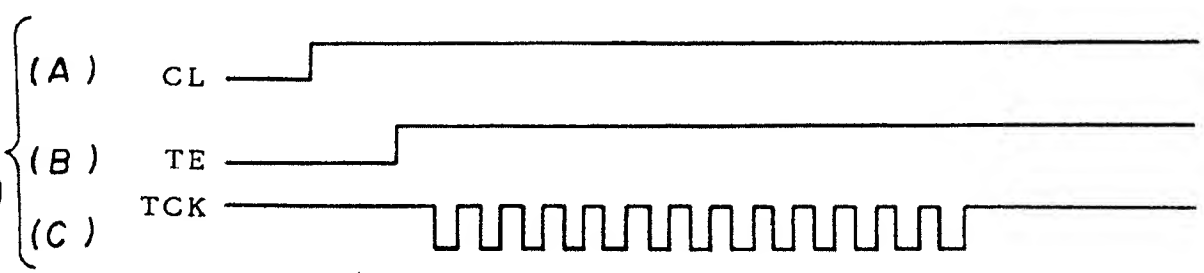

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FIG.3A (PRIOR ART)

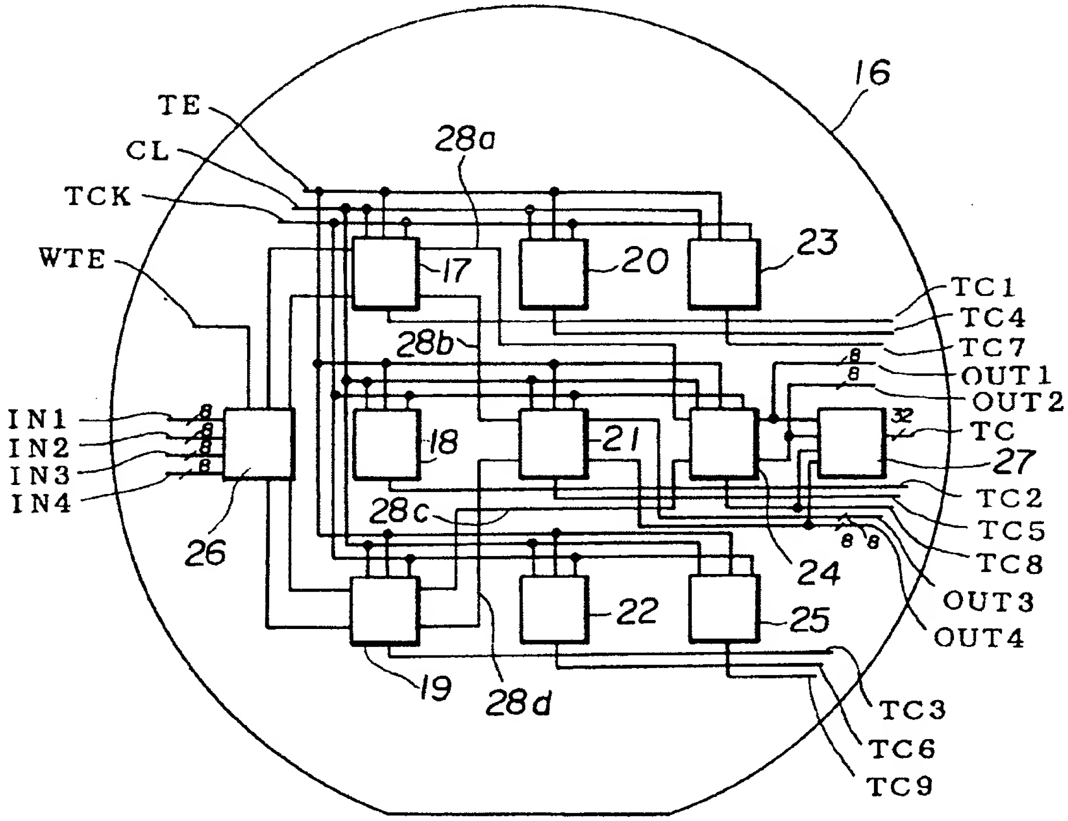


FIG.3B (PRIOR ART)

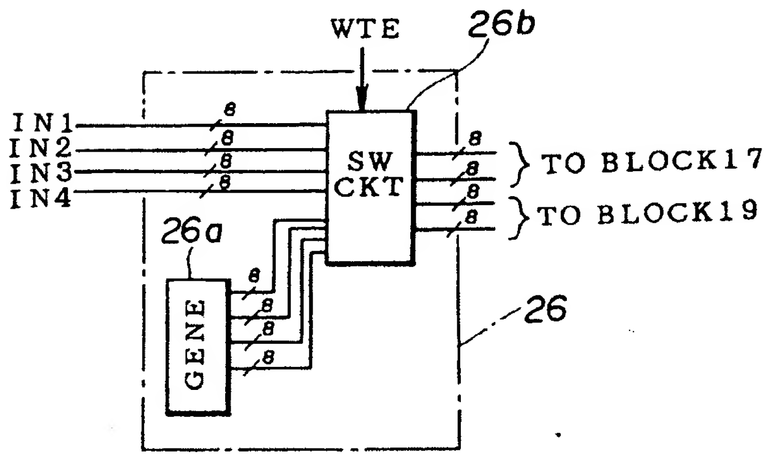
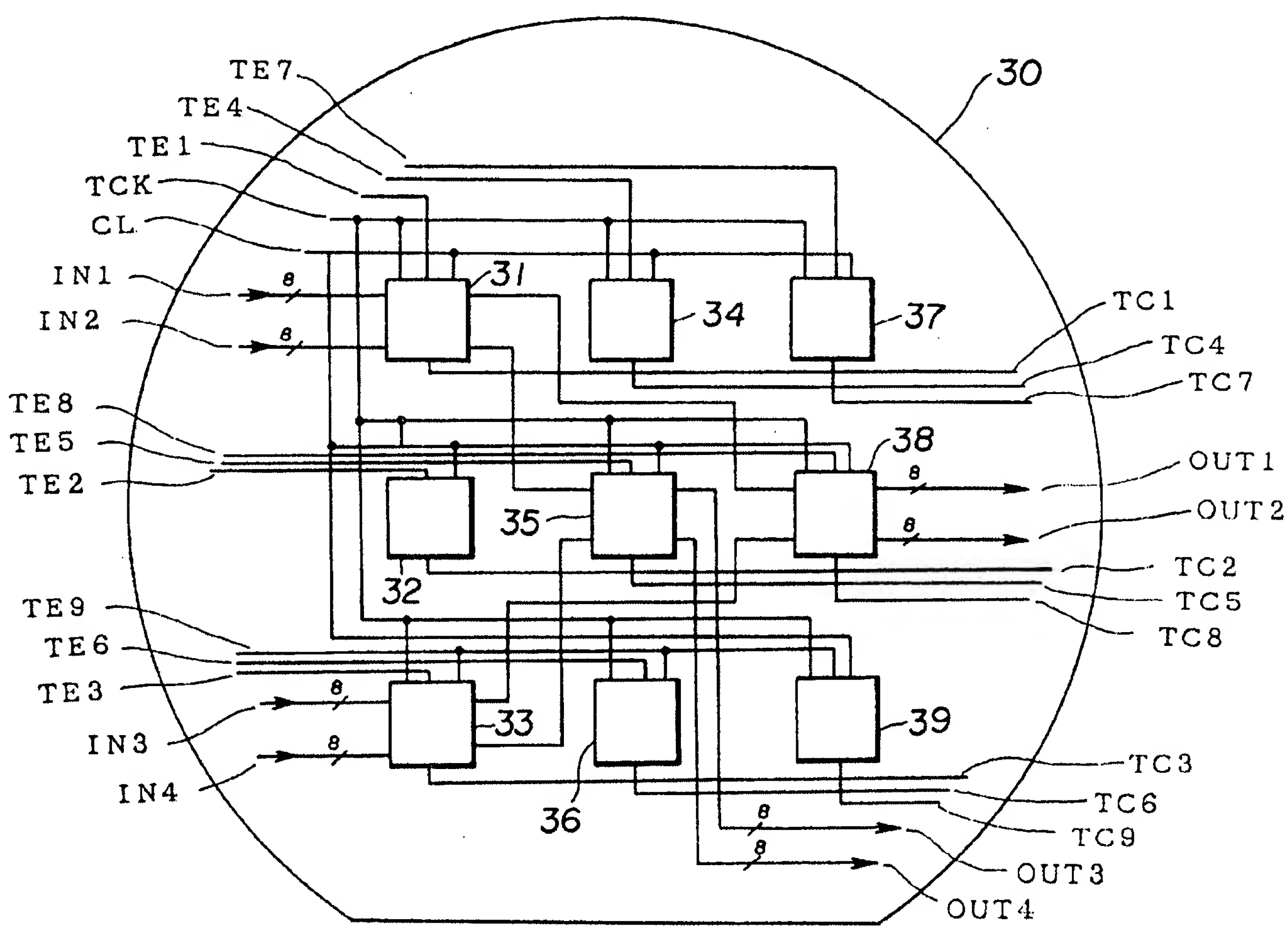
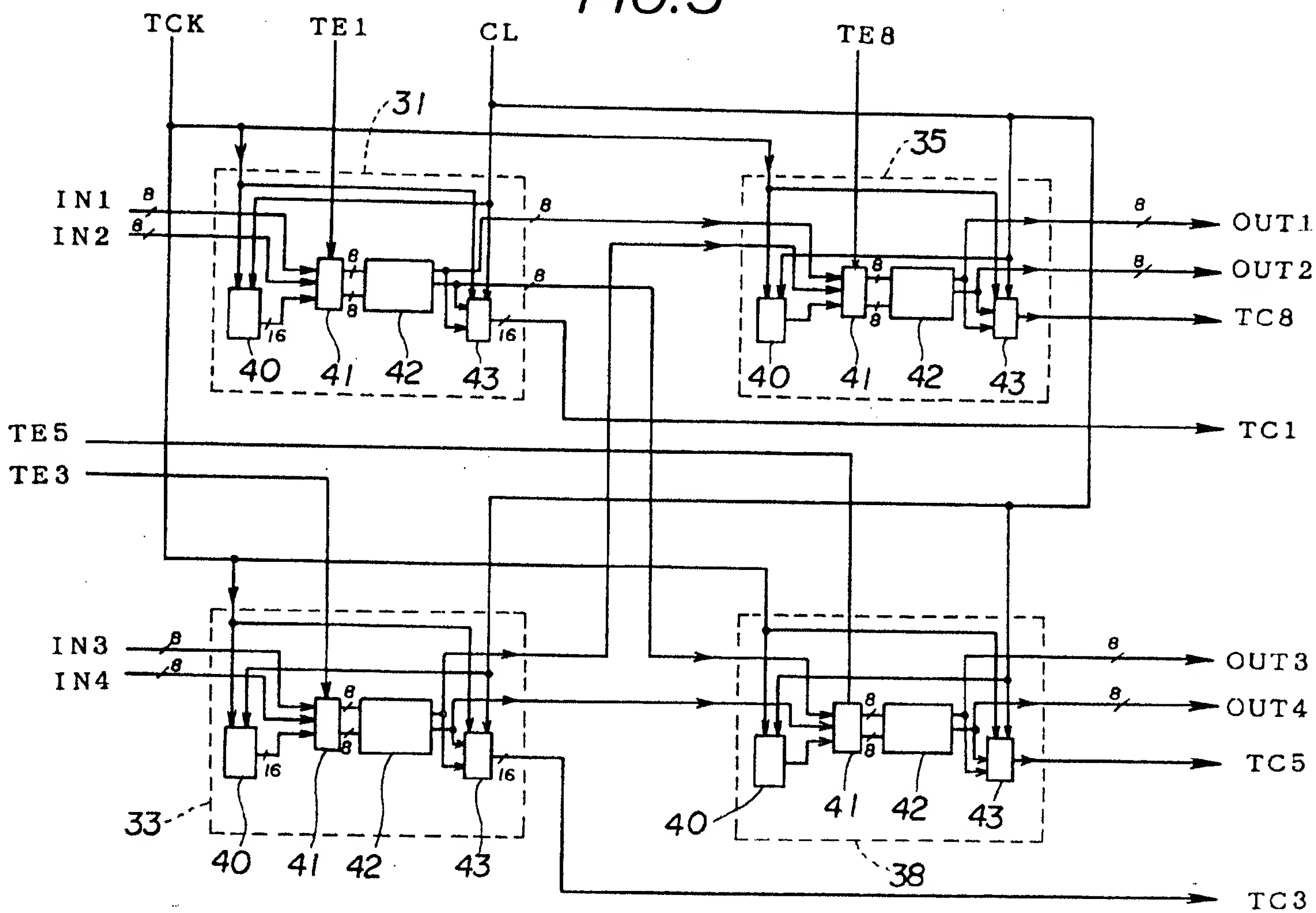


FIG.4



30
TE7
TE4
TE1
TCK
CL
IN1
IN2
TE8
TE5
TE2
TE9
TE6
TE3
IN3
IN4
31
32
33
34
35
36
37
38
39
8
TC1
TC4
TC7
OUT1
OUT2
TC2
TC5
TC8
TC3
TC6
TC9
OUT3
OUT4

FIG.5



TCK
TE1
CL
TE8
31
35
IN1
IN2
8
16
40
41
42
43
OUT1
OUT2
TC8
TC1
TE5
TE3
IN3
IN4
33
38
OUT3
OUT4
TC5
TC3

FIG.6

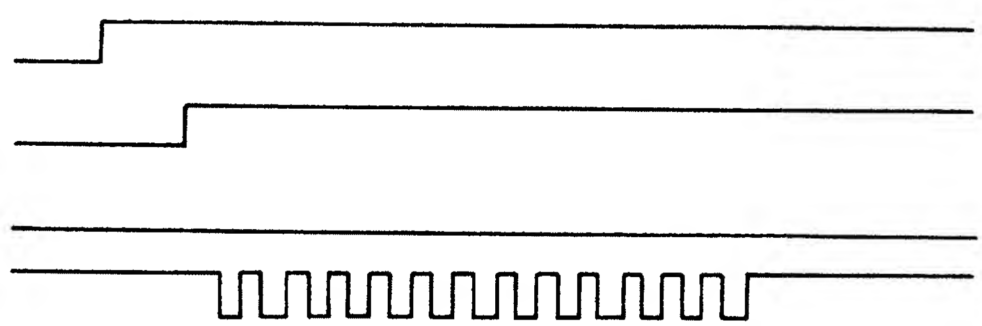


FIG.9

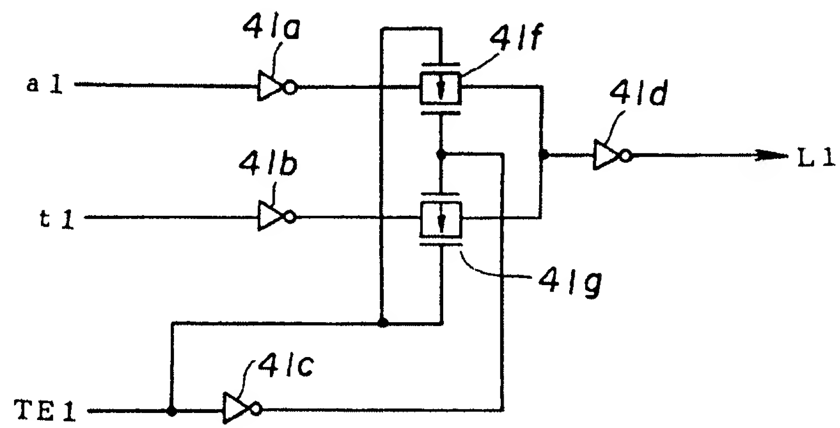


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FIG. 7

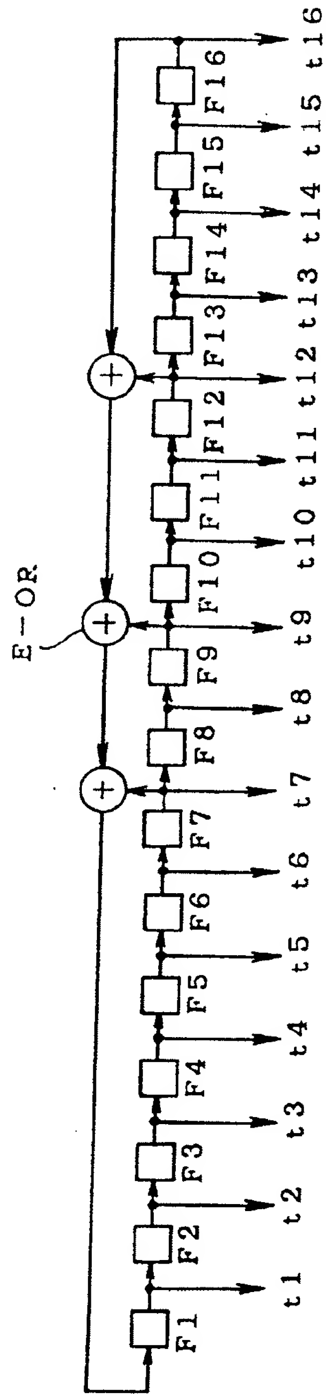


FIG. 10

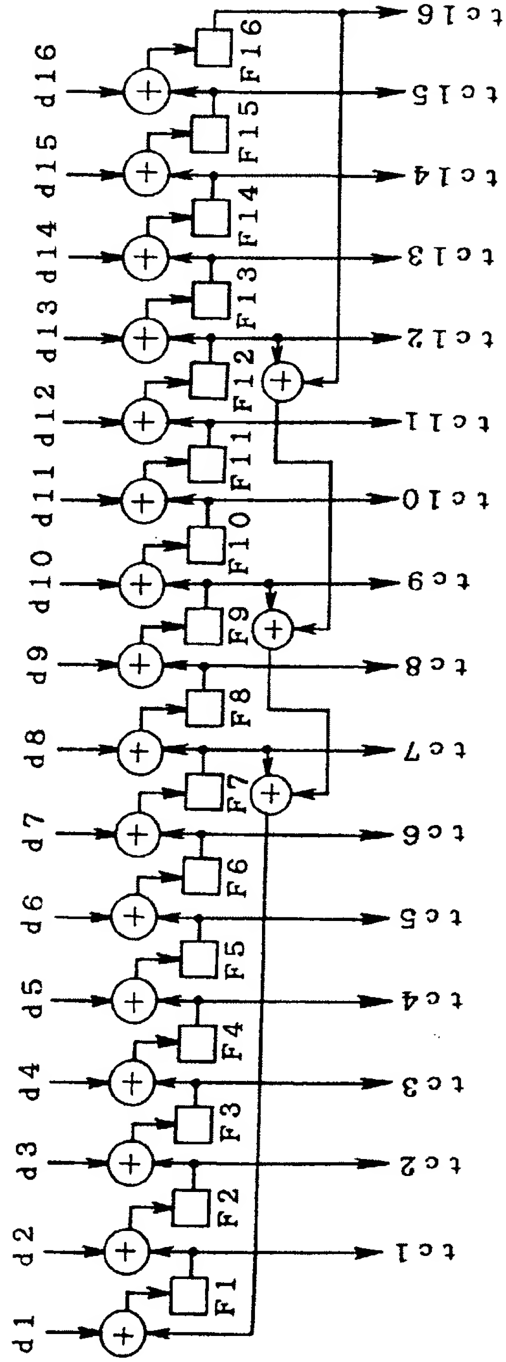
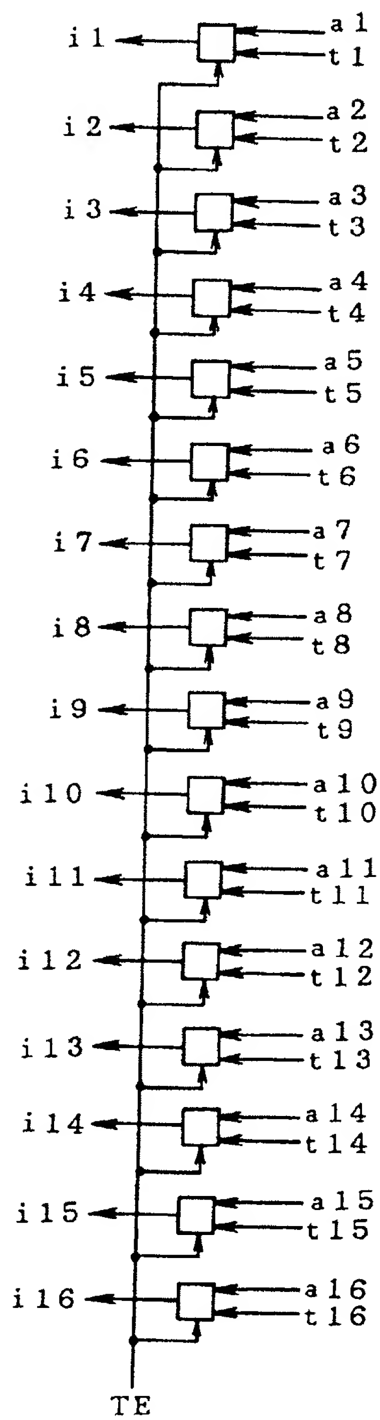


FIG.8


i 1
a 1
t 1
i 2
a 2
t 2
i 3
a 3
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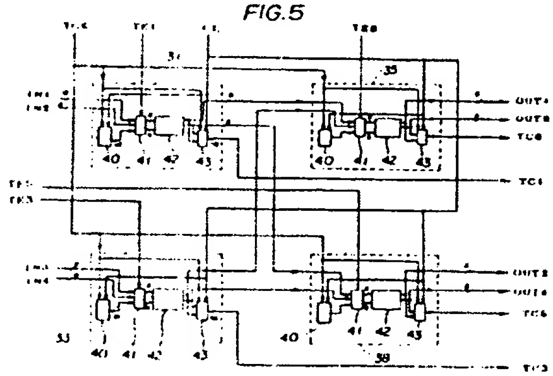
(54) Semiconductor integrated circuit with a test function.

(57) A semiconductor integrated circuit comprises a plurality of integrated circuit blocks (31 - 39) constituted on a wafer (30), the integrated circuit blocks being arbitrarily electrically connected to each other so as to form a system. Each of the integrated circuit blocks comprises a logical operating circuit (42) for carrying out a logical operation; a pseudo-random pattern generating circuit (40) for generating a pseudo-random pattern signal; switching circuit (41) for selecting either an input signal to be processed by the logical operating circuit or the pseudo-random pattern signal in response to a test enabling signal (TE1 - TE9) which is independently applied to each integrated circuit block so that each integrated circuit block is independently set to either a test mode or a normal mode and for outputting the selected signal to the logical operating circuit; and a data compressing circuit (43) for compressing an output data signal of the logical operating circuit.

FIG.5



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EUROPEAN SEARCH REPORT

Application Number

EP 87 40 2872

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Y	ELECTRONIC DESIGN, vol. 33, no. 16, 11th July 1985, pages 63-64, Schiphol, NL; M. BEEDIE: "Testing, fault tolerance emerge as top issues at wafer-scale conference" * Page 63, column 1, last paragraph - column 2; page 64, column 2, lines 39-46 *	1,3,4	G 01 R 31/28
A	* Page 63, column 3, lines 28-40 *	6	
Y	AUTOTESTCON'80-1980 AUTOTEST CONFERENCE, Washington, 2nd-5th November 1980, pages 135-139, IEEE, New York, US; D.K. BHAVSAR; "Self-testing supercells" * Page 138, paragraph "Polynomial division (POLYDIV) Scheme" *	1,3,4	
A	* Page 138, point "FSR" *	7	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
P,X	PROCEEDINGS OF THE IEEE 1987 CUSTOM INTEGRATED CIRCUITS CONFERENCE, Portland, 4th-7th May 1987, pages 207-210, IEEE, New York, US; K. YAMASHITA et al.: "A wafer-scale 170,000-gate FFT processor with built-in test circuits" * Whole article *	1-7	G 06 F 11/26 G 01 R 31/28 G 06 F 11/20

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12-12-1989	SARASUA GARCIA L.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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